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U.S. UTILITY Patent Application

PATENT NUMBER and
ISSUE DATE

APPL NUM 10092310	FILING DATE 03/07/2002	CLASS 430	SUBCLASS 27	GAU 1752	EXAMINER W. J. ...
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**APPLICANTS: Ooturo Akihiko; Takechi Satoshi;

**CONTINUING DATA VERIFIED: *none*

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** FOREIGN APPLICATIONS VERIFIED: *none*
JAPAN 2001-180584 06/14/2001

PG-PUB. DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>
Foreign priority claimed <input checked="" type="checkbox"/> yes <input type="checkbox"/> no	ATTORNEY DOCKET NO
35 USC 110 conditions met <input checked="" type="checkbox"/> yes <input type="checkbox"/> no	020201
Verified and Acknowledged Examiners's initials <i>[Signature]</i>	
TITLE : Multi-layered resist structure and manufacturing method of semiconductor device	

U.S. DEPT. OF COMM./PAT. & TM. PTO-436L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
ISSUE FEE		DRAWING	
Amount Due	Date Paid	Sheets Drawg.	Figs. Drawg.
		Print Fig.	
<input type="checkbox"/> TERMINAL DISCLAIMER		Primary Examiner PREPARED FOR ISSUE Application Examiner	
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